1. (Amended) A semiconductor device comprising:

a die pad;

a die pad supporter which supports said die pad;

a plurality of inner leads arranged to surround said die pad; and

a semiconductor chip which has a size larger in area than that of said die pad and which is mounted on said die pad;

wherein said die pad supporter has a stress absorbing portion which is located between said die pad and ends of said inner leads,

wherein said semiconductor chip is disposed over the stress absorbing portion, and

wherein a part of said die pad supporter is located between a pair of said inner leads and extends along the pair of said inner leads.

5. (Amended) A semiconductor device comprising:

a die pad;

a die pad supporter which supports the die pad;

a plurality of inner leads arranged to surround the die pad; and

a semiconductor chip which has a size larger in area than that of said die pad and which is mounted on said die pad;

wherein said die pad supporter has a first portion, a pair of second portions, and a pair of third portions, wherein said first portion is disposed between a pair of said

inner leads and extends along the pair of said inner leads, and wherein one end of each of said second portions connect to one end of said first portion, and said each of said second portions extend in a direction different from a direction in which said first portion is extended, and wherein one end of each of said third portions each connects to another end of respective said second portions and another end of each of said third portions are connected to the die pad.

6. (Amended) A semiconductor device comprising:

a die pad;

a die pad supporter which supports the die pad;

a plurality of inner leads arranged to surround the die pad; and

a semiconductor chip which has a size larger in area than that of said die pad and which is mounted on said die pad;

wherein said die pad supporter includes a frame portion which has a rectangular shape, a first portion connected between a side portion of said frame portion and the die pad, and a second portion which extends from a corner portion of said frame portion to between a pair of said inner leads, and wherein the frame portion and the first portion are disposed between the inner leads and the die pad.

7. (Amended) A semiconductor device according to claim 6, comprising a plurality of said second portions, wherein each of said second portions is disposed

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between said inner leads and disposed substantially parallel with said inner leads adjacent to the second portions.

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9. (Amended) A semiconductor device according to claim 6, wherein said semiconductor chip has a first surface on which an integrated circuit is formed and a second surface which is opposite said first surface, and wherein said frame portion is arranged adjacent the second surface of the semiconductor chip.

10. (Amended) A semiconductor device comprising:

a die pad;

a plurality of inner leads arranged to surround the die pad;

a semiconductor chip which has a size larger in area than that of said die pad and which is mounted on said die pad;

a frame portion which substantially surrounds the die pad and is disposed between said inner leads and said die pad;

first die pad supporters each of which supports the frame portion from four directions; and

a second die pad supporter which connects the frame portion and said die pad;

wherein said second die pad supporter is extended along a direction different from directions in which the first die pad supporters are extended.

11. (Amended) A semiconductor device according to claim 10, wherein said semiconductor chip is disposed on the frame portion.

12. (Amended) A semiconductor device according to claim 11, wherein said first die pad supporters and said second die pad supporter are staggered at the frame portion.

13. (Amended) A semiconductor device according to claim 10, wherein said frame portion has substantially rectangular shape, and wherein said first die pad supporters each support substantially corner portions of said frame portion, and wherein said second die pad supporter connects at a side portion of said frame portion.

Please add claims 14-22 as follows:

--14. A semiconductor device according to claim 1, wherein said die pad supporter has a down-set portion which is located at an area between the pair of said inner leads.

15. A semiconductor device according to claim 5, wherein said first portion of said die pad supporter has a down-set portion which is located at an area between the pair of said inner leads.

16. A semiconductor device according to claim 6, wherein said second portion of said die pad supporter has a down-set portion which is located at an area between the pair of said inner leads.

17. A semiconductor device according to claim 10, wherein said first die pad supporters have a down-set portion which is located at an area between respective pairs of said inner leads.

18. A semiconductor device according to claim 1, wherein said stress absorbing portion includes a slit formed in said die pad supporter.

19. A semiconductor device according to claim 1, wherein said stress absorbing portion has a protruding portion and a concave portion which corresponds to the protruding portion.

20. A semiconductor device according to claim 1, wherein said stress absorbing portion has an S-shaped configuration.

21. A semiconductor device according to claim 1, wherein said part of said die pad supporter extends substantially in a direction parallel to the pair of said inner leads.

22. A semiconductor device according to claim 5, wherein said first portion of said die pad supporter extends substantially in a direction parallel to the pair of said inner leads.--